

1      ABSTRACT OF THE DISCLOSURE

2      A static random access memory cell comprising a first inverter  
3      including a first p-channel pullup transistor, and a first n-channel  
4      pulldown transistor in series with the first p-channel pullup transistor;  
5      a second inverter including a second p-channel pullup transistor, and a  
6      second n-channel pulldown transistor in series with the second n-channel  
7      pullup transistor, the first inverter being cross-coupled with the second  
8      inverter, the first and second pullup transistors sharing a common active  
9      area; a first access transistor having an active terminal connected to the  
10     first inverter; a second access transistor having an active terminal  
11     connected to the second inverter; and an isolator isolating the first  
12     pullup transistor from the second pullup transistor.

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